SN76430N COLOR GENERATOR IC

FEATURES

- Provides color composite video signal.
- Produces horizontal and vertical sync pulses.
- Built-in video summing section.

CIRCUIT DESCRIPTION

The SN76430N utilizes low-power Schottky TTL technology to provide a color composite video output signal, video summing, and horizontal and vertical synchronization pulses in a complete video game system. Clock reference is a 3.58 MHz crystal. Of course, the chip is TTL and CMOS compatible. Block diagram for SN76430N chip is shown in Fig. 6-14.

IC OPERATION

The circuit generates horizontal and vertical sync pulses from a 3.58 MHz internal oscillator. The chip also contains a video summer accepting video information from five video inputs (pins 16, 17, 18, 19, and 20). A composite video waveform is generated containing horizontal and vertical blanking, horizontal and vertical sync, color burst background video information, spot video information (players, walls, balls, score, etc.), and serration pulses.

Color burst begins at the end of horizontal sync and continues for 14 cycles of the subcarrier (3.58 MHz), and is present on all lines except those where serration pulses are present. The color yellow is assigned to any information fed to video inputs 16

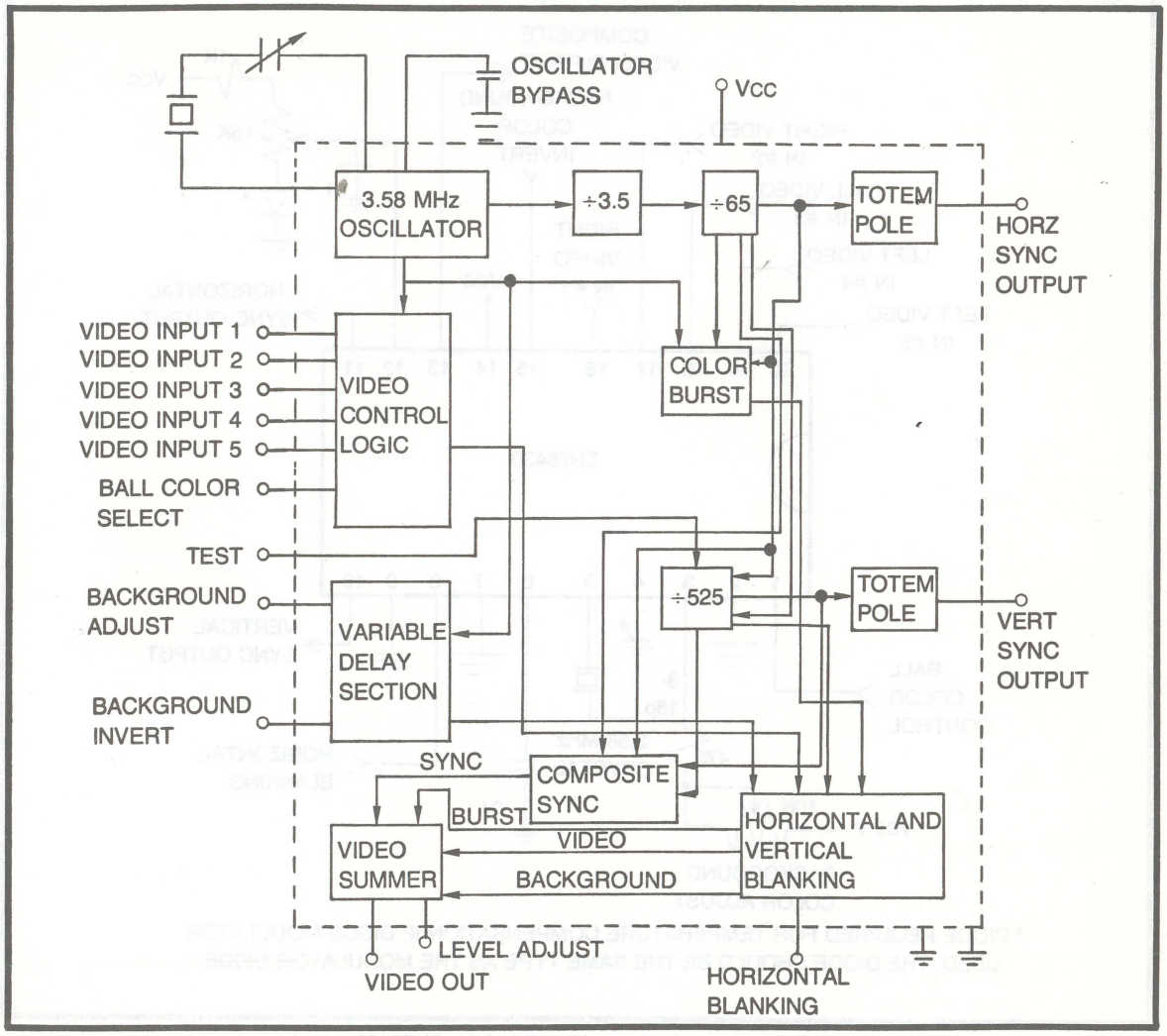

Fig. 6-14. Block diagram for the SN76430N IC.

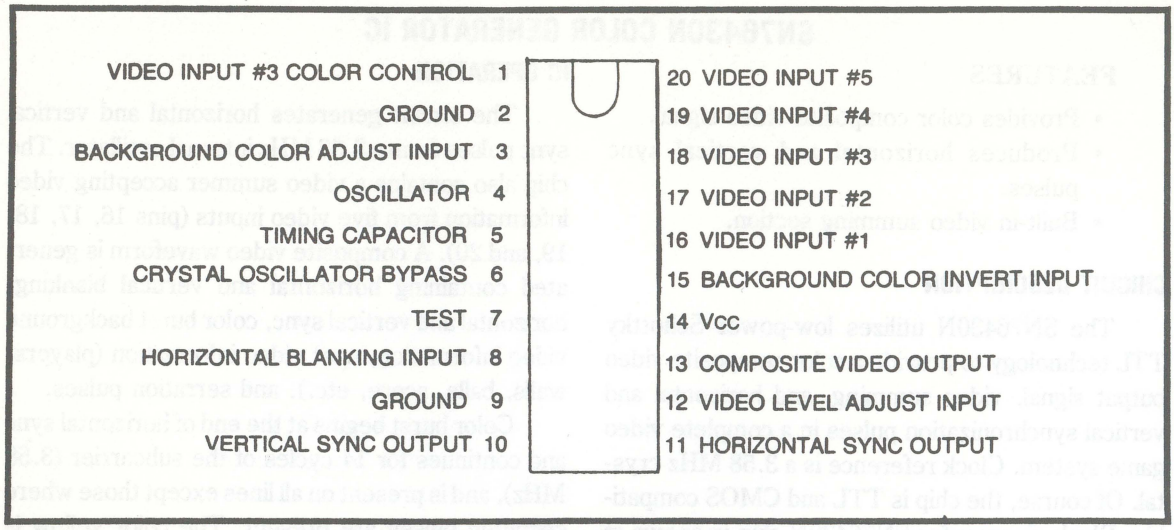

Fig. 6-15. SN76430N IC pin assignment.

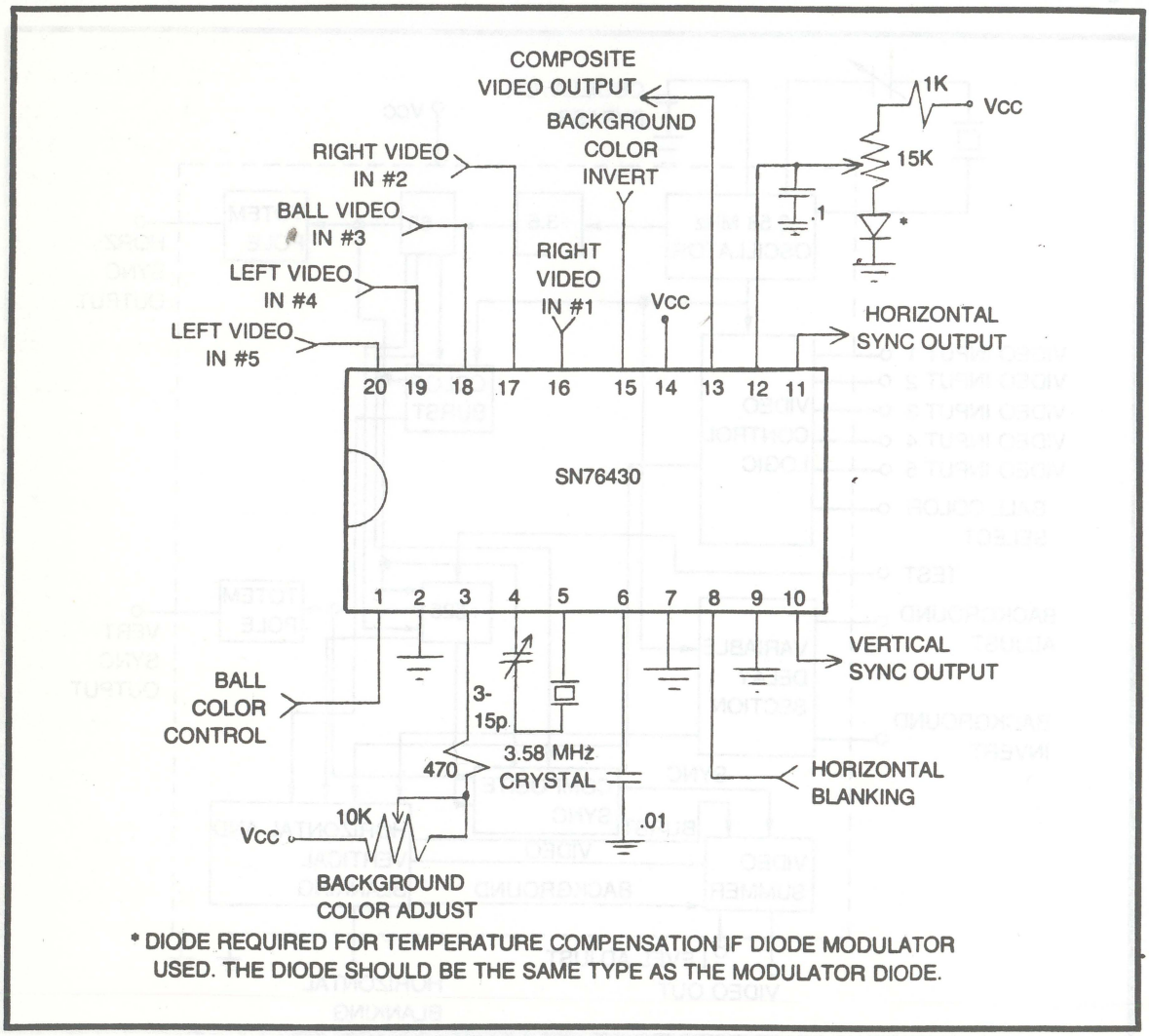

Fig. 6-16. Application schematic of the SN76430.

and 17. The color phase is the same as burst. Light-blue color is assigned to any information fed to video input pins 19 and 20. The information fed to pin 18 is yellow when pin 1 is a logic *zero*, matching the yellow assigned to pins 16 and 17. When pin 1 is switched to a logic *one*, the information at 18 is changed to the light-blue color, matching the light-blue color assigned to pins 19 and 20.

Background color is adjustable by raising or lowering the DC level into pin 3, with an adjustment of about 180° possible. A background color inversion of 195° from pin 3 setting may be obtained by applying a logic *one* to the background color invert pin (pin 15).

Horizontal and vertical sync outputs are totem-pole type, and compatible with standard TTL and CMOS circuits. Horizontal sync pulse width is approximately 4.85 μs. Vertical sync pulse width is three horizontal sync pulses. Vertical blanking begins 3 horizontal lines before vertical sync, and continues for 19 horizontal lines. Horizontal blanking (generated externally, and applied at pin 8) and vertical blanking will eliminate video signals, excluding burst.

Refer to Fig. 6-15 for pin assignment of SN76430N chip. A typical game application schematic for the SN76430N IC is shown in Fig. 6-16.

SN76431N IC DUAL OSCILLATOR

The SN76431N is a low-power TTL compatible IC containing all of the circuitry required to provide two oscillator clocks for controlling the horizontal and vertical positions of two complex characters used in some TI game circuits. Note block diagram in Fig. 6-17.

CHIP OPERATION

The frequency of each oscillator is determined by the RC network at pins 7 and 11. Pin 7 is the frequency adjust for oscillator 1 and pin 11 is the frequency adjust for oscillator 2. When used with the complex character circuits, a 1.5 MHz output frequency is required. The RC values for this output are shown in the typical application schematic shown in Fig. 6-18.

The horizontal position of the characters are determined by where the oscillators are turned on during each line of horizontal scan, gating the complex character circuit. The oscillator-on position

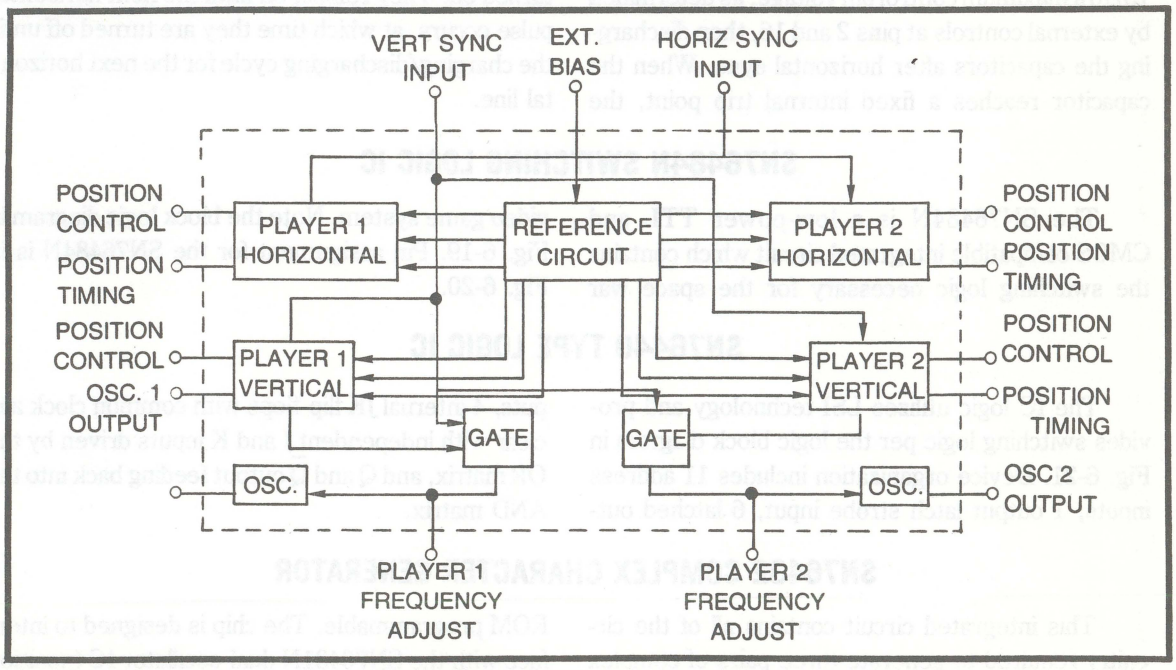

Fig. 6-17. Block diagram of the SN76431N IC.